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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,020	03/19/2004	Hun Jeoung	8733.1043.00-US	6997

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EXAMINER	
KIM, RICHARD H	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,020	JEOUNG, HUN	
	Examiner	Art Unit	
	Richard H. Kim	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *1-16 and 21-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-20* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17 and 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,310,670 B1) in view of Toyota et al. (US 2002/0154252 A1) and Nakamura et al. (US 5,245,452).

Referring to claim 17, Lee discloses a method comprising forming a semiconductor layer, a drain electrode (abstract), and a pixel electrode (120) on a substrate using doped (p-type, n-type) polycrystalline silicon (col. 6, lines 15-17), the semiconductor layer including an active area (col. 5, lines 56) and a source area (56a); forming a gate insulating layer (54), a gate line (100), a common electrode (110), wherein forming a gate insulating layer, a gate line, a common electrode including forming a first insulating layer (54) and a first metal layer (66) on the substrate including the semiconductor layer, the drain electrode and the pixel electrode; patterning the first insulating layer and the first metal layer, wherein the gate line overlaps the active area of the semiconductor layer (Fig. 4, ref. 100; Fig. 9, ref. 66, 56); forming an inter insulating layer (68) to cover the gate line and the common electrode by forming a second insulating layer and patterning the second insulating layer, the inter insulating layer having a source contact hole (70) to expose the source area; and forming a data line (105) on the inter insulating layer, wherein forming the data line included forming and patterning a second metal

layer, the data line being connected to the source area through the source contact hole (125). However, the reference does not disclose a first capacitor electrode of polycrystalline silicon and a second capacitor electrode, the second capacitor electrode covers the first capacitor electrode, and a common electrodes extends from a common line and a pixel electrode of doped (n-type or p-type) polycrystalline silicon.

Toyota et al. discloses a first capacitor of polycrystalline silicon (14) and a second capacitor (8), the second capacitor electrode covers the first capacitor electrode. Nakamura et al. discloses a method of using a pixel electrode of doped (n-type or p-type) polycrystalline silicon (col. 4, lines 60-61).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a first capacitor electrode of polycrystalline silicon and a second capacitor electrode since one would be motivated to increase contrast by improving the capacitance of the storage electrodes (paragraph 0009). Moreover, it would have been obvious to one having ordinary skill in the at the time the invention was made to employ a pixel electrode of doped (n-type or p-type) polycrystalline silicon since one would be motivated to prevent avoid problems regarding the resistance of the electrode (col. 5, lines 32-33). Furthermore, common lines are well known in the art to provide a common signal to the common electrode.

Referring to claim 20, Lee, Toyota et al. and Nakamura et al. disclose the device previously recited. However, the references do not disclose masking the active are of the semiconductor layer and doping the source area of the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to mask the active are of the semiconductor layer and dope the source area of the semiconductor layer, the drain electrode, the first capacitor electrode and the pixel electrode since using such a method to prevent from doping a certain region is well known in the art to efficiently dope selected regions.

3. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, Toyota et al. and Nakamura et al. in view of Murade et al. (US 6,480,244 B2).

Lee, Toyota et al. and Nakamura et al. disclose the method previously recited, but fails to disclose that the first capacitor is n-type or p-type doped.

Murade et al. discloses a method wherein the capacitor is n-type or p-type doped (col. 14, lines 350-39).

It would have been obvious to one having ordinary skill in the art to employ a method wherein the capacitor is n-type or p-type doped since one would be motivated to for a capacitor of low resistance (col. 14, lines 37-38).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard H. Kim whose telephone number is (571)272-2294. The examiner can normally be reached on 9:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard H Kim
Examiner
Art Unit 2871

RHK

ANDREW SCHECHTER
PRIMARY EXAMINER